Code No: C2EC02 **N5-05**

**II B.Tech.(CCC) Supplimentary Examinations, June 2008**
**PULSE DIGITAL AND SWITCHING CIRCUITS**
**(Electronics & Communication Engineering)**

**Time: 3 hours** **Max Marks: 100**

**Answer any FIVE Questions**
**All Questions carry equal marks**

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1. (a) A square wave whose peak-to-peak value is 1V extends ± 0.5 V with respect to ground. The duration of the positive section is 0.1 Sec and of the negative section is 0.2 sec. If this wave form is impressed up on an RC differentiating circuit whose time constant is 0.2 sec; what are the steady state maximum and minimum values of the output waveform? [12]

   (b) Prove that the area under the positive section is equal to the area under the negative section of the output waveform of a high- pass RC circuit. [8]

2. (a) Give the circuits of series clipper circuits and explain their operation with the help of transfer characteristics. [10]

   (b) For the circuit shown in the figure 2b : sketch the input and output waveforms if R = 1 KΩ [10]

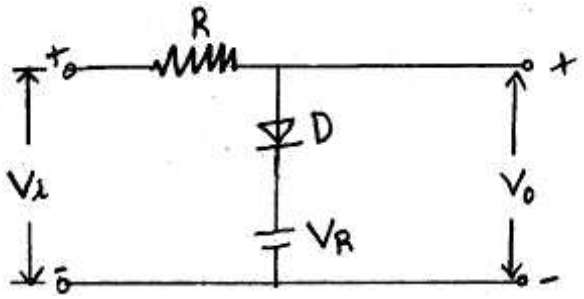


Figure 2b

$V_R$ = 10 V, $V_i$ = 20 Sin $\omega$t
$R_f$ = 100 Ω $R_r$ =$\propto$
$V_\gamma$ = 0

3. (a) Draw the circuit diagram of an astable multi and explain its operation. [12]

   (b) A collector-coupled astable multi uses n-p-n transistors with $h_{FE}$(min)=30.The parameter values are:
   $R_1 = R_2$= 50 KΩ and $C_1 = C_2$ = 0.1 $\mu$F and $V_{CC}$ = 10V.
   Find the pulse width, period and frequency of the output. [8]

4. Explain the operation of free running blocking oscillator (diode controlled) with neat sketch of current and voltage waveforms. Derive the expression for period and duty cycle of oscillations. [20]

5. (a) Write the following binary numbers in signed 1's complement form and signed 2's complement form using 16 bit registers.

i. +1001010
ii. -11110000
iii. -11001100.1
iv. +100000011.111

(b) Perform N1+N2,N1+(-N2) for the following 8 bit numbers expressed in a 2's complement representation. Verify your answers by using decimal addition and subtraction. [12+8]

i. N1=00110010, N2=11111101
ii. N1=10001110, N2=00001101

6. Using the tabular method, obtain the prime implicants of a four- input single-output function f(w,x,y,z) = $\sum$m(0,2,4,5,6,7,8,9,10,11,13). Reduce the prime-implicant table and find the minimal cover of f. [20]

7. (a) Draw and explain with the help of truth table the logic diagram of a master slave D flip-flop using NAND gates. With active low preset and clear and with negative edge triggered clock.

(b) Give the transition table for RS flip flop.

(c) Convert JK flip flop into T and D flip flops. [10+2+8]

8. For the machine shown in table, find a minimum state reduced machine containing the original one [20]

| PS | NS,Z | |
|---|---|---|
| | $I_1$ | $I_2$ |
| A | - | F,0 |
| B | B,0 | C,0 |
| C | E,0 | A,1 |
| D | B,0 | D,0 |
| E | F,1 | D,0 |
| F | A,0 | |

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