Wide bandgap semiconductor materials for high temperature electronics

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Abstract

High temperature electronics is an advancing field aimed at the development of semiconductor devices designed to function reliably at temperatures in excess of 125°C. Already conventional semiconductor materials like silicon or gallium arsenide are capable of operating to 300–400°C using 'temperature hardening' modifications in design and associated materials such as metallisation schemes. Despite this progress a significant body of research has been focused towards the development of wide bandgap semiconductor materials. These are semiconductors with bandgaps larger than those of Si (1.1 eV) and GaAs (1.43 eV) and include silicon carbide (3C 2.39 eV, 6H 3.02 eV); the I III-nitride (In0.53Al0.47As), Ga0.72N, N alloys (0 ≤ x, y ≤ 1) with band gaps ranging from 1.9–6.2 eV; and diamond (5.45 eV). The wider bandgap potentially offers higher operating temperatures before the thermally activated intrinsic carrier current causes latch up. This paper reviews the current status of wide bandgap semiconductor material growth and semiconductor doping. Examples of high temperature devices fabricated from these materials, their processing and electrical characteristics are discussed. © 1999 Elsevier Science S.A. All rights reserved.

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1. Introduction

There is a growing trend towards the deployment of electronics in high temperature environments. This is a response to the growing demands for intelligent control systems across a wide range of technological applications. For a number of years a rather artificial upper limit of 125°C was set by military specifications for conventional components and systems to withstand. Within the last decade it has emerged that engineers have broken this glass ceiling by modifying off the shelf technology with packaging, solders, interconnects and substrates able to function for a few tens or even hundreds of hours above 125°C. This has been particularly true in the field of oil and gas exploration [1] where the benefit of maintaining a bore hole logging tool for slightly longer or at lower depths might reap enormous economic benefits.

High temperature electronics are also attractive for possible applications in automotive or aerospace engine control units [2] and other distributed control scenarios where they might bring the benefits of higher reliability and safety, reduced fuel consumption and lower noxious emissions. The same type of arguments can be made for any application where smart microsystem technologies can play a role in high temperature environments. All of these driving forces have provided the motivation to develop new electronic materials for high temperatures rather than adapt the conventional semiconductor workhorses such as silicon and gallium arsenide.

The failure of semiconductors at high temperatures is due to either (i) dramatic changes in electrical characteristics so that the circuit design parameters are not met or (ii) material changes such as interdiffusion or corrosion occur in the device causing loss of function. A significant factor influencing the first category of failure is the dependence of intrinsic carrier concentration on temperature which causes threshold voltage shifts and leakage currents leading to degraded device characteristics initially and eventually the latch-up phenomenon [3]. When the semiconductor atoms yield thermally generated carrier pair concentrations exceeding those contributed by the extrinsic impurity dopants the material becomes intrinsic. Pure silicon has valence and conduction band densities of states of 1.04 × 10^{10} and 2.8 × 10^{19} cm⁻³, respectively [4]. For impurity doped silicon at the level of 5 × 10^{14} cm⁻³ this yields and extrinsic-intrinsic transition point at about 275°C. Depending on the doping regime bulk silicon electronics will operate at slightly higher temperatures and have the benefits of manufacturing scale, yield and reliability which all influence economics. However the relatively narrow bandgap of silicon means that thermal ionisation of intrinsic carriers limits the operation of bulk silicon devices to below 300°C in practice.

The strategies adopted to minimise these effects include
the use of dielectric isolation or silicon-on-insulator (SOI) which eliminates parasitic leakage currents between devices and the formation of parasitic devices. The current state of the art [3] is that SOI devices can be functional above 300°C for extended periods. Another alternative to use semiconductors with a wider bandgap, such as gallium arsenide, or the more recent wide bandgap semiconductors such as silicon carbide, the III-nitrides or diamond. Fig. 1 compares the intrinsic carrier concentration of silicon with other wider bandgap semiconductors and summarises some of the major electronic materials transitions that occur across this temperature range. High temperature operation of silicon grown on insulators have been demonstrated up to 400°C, and this field has been recently reviewed by Hartnagel [6] and Klein [7]. This paper reviews the current state of wide bandgap semiconductor materials for high temperature electronics.

2. Silicon carbide

2.1. Silicon carbide growth and doping

Silicon Carbide high temperature electronics research is probably the most well established of the three classes of wide bandgap semiconductor materials reviewed here. Key research issues associated with SiC electronics include control of crystalline structure and defects in the semiconductor material; suppression of the background intrinsic carrier concentrations and p-type doping; minimisation of dry etching damage in the formation of device structures; and formation of the complimentary oxide with sufficiently low interface carrier densities.

Two significant factors in SiC growth are polytypism and the formation of micropipe defects. Polytypism is a form of one dimensional polymorphism in which the crystalline structure of individual polytypes is determined by the periodicity of tetrahedrally bonded Si–C layers that make up the SiC lattice. These tetrahedra can be stacked in a series of layers which gives rise to the generic polytypes.

The zinc blende phase is metastable with respect to the wurtzite phase. Silicon carbide exhibits some 200 polytypes with unique electronic structure which determines their semiconducting properties. At either extreme are the completely cubic structure 3C- or 6H-SiC which has a bandgap of 2.3 eV and the wurtzite structure which is termed 2H-SiC (a member of the α-SiC group) which has a bandgap of 3.3 eV. Other common polytypes of technological interest are 4H- and 6H-SiC. Some rhombohedral phases are also known for example, the 15R- and 21R-SiC polytypes. Growth parameters such as substrate temperature, flux composition and arrival rate have to be carefully controlled in order to achieve adequate phase purity for electronic grade material.

The issue of micropipes in the SiC bulk material is an enduring one. Micropipes are voids that propagate through the length of a boule and densities of the order of $10^8 \text{cm}^{-3}$ or more are still common [8]. Probably the most commercially significant SiC production method is the modified Lely process [9–11] which is able to grow larger SiC single crystals by introducing a significant temperature gradient between the source materials and the seed. In this way, it has been possible to grow large crystals of a single polytype (4H, 6H and 15R) with diameters of about 15–20 mm and about the same height at growth rates of the order of mm/h.

The bulk silicon carbide material is frequently combined with higher purity homoepitaxial layers to produce electronic grade materials and this has stimulated extensive research into heteroepitaxial silicon carbide deposition on relatively inexpensive substrates such as silicon. The sublimation method has been used to deposit homoepitaxial films via the ‘sandwich method’ of Vodakov et al. [12]. 6H and 4H layers have been grown with contamination levels of below $10^{10} \text{cm}^{-2}$ and dislocation densities of less than $10^6 \text{cm}^{-2}$.

Chemical vapour deposition has also been used for the production of SiC homoepilayers as well as for heteroepitaxial processes. The Nishino process [13] provides a benchmark for heteroepitaxial processes and has been widely employed since the mid-1980’s as a means of depositing β-SiC onto silicon at relatively high substrate temperatures (1360°C). The large lattice mismatch between SiC and Si (about 20%) is ameliorated via a silicon carbide buffer layer formed by carburising the silicon surface. Subsequently, large-area heteroepitaxial β-SiC films can be deposited on silicon substrate using a feedstock of silane and propane. The layers produced by this method typically contain high densities of defects such as microtwins, intrinsic stacking faults and inversion domain boundaries (IDBs) [14].

Low temperature CVD processes have been investigated using alternative precursors to promote dissociation at lower substrate temperatures. These have included halogenated silicon molecules and Si-C directly bonded precursors.
Table 1
High temperature silicon carbide devices and characteristics

<table>
<thead>
<tr>
<th>Material</th>
<th>Type/Mode</th>
<th>Gate length (μm)</th>
<th>g_m (mS/mm)</th>
<th>Mobility (cm²/V s)</th>
<th>Upper operating temp (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3C-SiC</td>
<td>MOS/depletion</td>
<td>2.4</td>
<td>10</td>
<td>37</td>
<td>750</td>
</tr>
<tr>
<td>3C-SiC</td>
<td>MOS/enhancement</td>
<td>5</td>
<td>0.46</td>
<td>Low</td>
<td>650</td>
</tr>
<tr>
<td>6H-SiC</td>
<td>JFET</td>
<td>5</td>
<td>17-20</td>
<td>250</td>
<td>627</td>
</tr>
<tr>
<td>6H-SiC</td>
<td>MOS/enhancement</td>
<td>7</td>
<td>2.8</td>
<td>46</td>
<td>450</td>
</tr>
<tr>
<td>6H-SiC</td>
<td>MOS/depletion</td>
<td>5</td>
<td>2.3</td>
<td>21</td>
<td>450</td>
</tr>
<tr>
<td>6H-SiC</td>
<td>MES</td>
<td>24</td>
<td>4.3</td>
<td>300</td>
<td>450</td>
</tr>
</tbody>
</table>

[15-19]. Atomic layer epitaxy (ALE) has also attracted some attention [20,21] and involves introducing the precursors in alternating pulses to develop the film structure layer by layer. Processes for depositing SiC epilayers on Si have currently been scaled to 100 mm wafer technology [22].

Intrinsic silicon carbide is usually n-type due to impurities in the source materials such as nitrogen which results in charge carrier densities typically between the order 10^{14} cm^{-3} [23]. Nitrogen is commonly employed as an extrinsic n-type dopant using ammonia or di-nitrogen precursors which yields up to ~10^{19} cm^{-3} carriers [24]. Compensation of the intrinsic carrier background has been reported with vanadium doping and ion implantation where it may act as an amphoteric impurity in SiC generating both deep donor and deep acceptor states [25-27].

P-type doping of SiC is complicated by the issue of over-compensating the intrinsic n-type background. Aluminium is widely used as a shallow p-type dopant for SiC using a trimethyl aluminium metalorganic precursor but boron may also be used. A significant step forward in silicon carbide doping has been reported [24,28] using a process termed as 'site-competition epitaxy'. The basis of the technique involves varying the Si/C ratio in the growth reactor to control the incorporation of the doping species, for example the N atoms onto C sites and Al atoms onto Si sites. By this method the p-doping range has been successfully extended over earlier reported limits by a further order of magnitude to 4 × 10^{19} cm^{-3}.

2.2. Silicon carbide high temperature devices

Morkoc et al [29] have reviewed some silicon carbide field effect transistors capable of functioning at high temperatures. Table 1 gives a subset of some of these studies and their main characteristics.

Scozzie et al [30] have characterised the electrical performance of 4H SiC depletion-mode junction field effect transistors (JFETs) over a temperature range from -55 to 400°C. The transistors design consisted of a buried gate and n-channel fabricated in epitaxial layers grown on bulk 4H-SiC wafers. The devices had a channel length of 5 mm and channel width 1 μm. The depth of the active channel region was 0.20 μm and the effective nitrogen donor concentration in the channel is 2.4 × 10^{17} cm^{-3}. The gate-side p-epilayer forming the junction with the channel region was doped to 1.6 × 10^{18} cm^{-3} and the 4H substrate was doped to 2 × 10^{18} cm^{-3} with aluminium acceptors. The current-voltage characteristics for these JFETs were modelled using standard abrupt-junction long-channel JFET equations. The model employed a two-level donor ionisation structure (0.050 and 0.080 eV) and assumed a two-step inverse power law dependence of mobility on temperature. The model results show close agreement with experimental data across the temperature range studied however deviations at the low temperature extreme was attributed to carrier freeze out and at the high temperature end to increased device leakage currents. The trade-off between controllable conductivity in the high temperature environment and effectively semi-insulator characteristics at ambient room temperatures or below is a significant issue for wide band gap semiconductors and will have to be incorporated into design schemes of high temperature electronic systems.

3. III-nitrides

3.1. Growth and impurity doping of III-nitrides

The application of III-nitride materials such as gallium nitride, aluminium nitride and the Al,Ga_{1-x},N alloys in high temperature electronics is in its infancy compared with silicon carbide but these materials have a long track record of research [31-36]. More recently the development of blue GaN light emitting diodes [37,38] and lasers have led to a dramatic surge of interest in the III-nitrides stimulated largely by Nakamura and his colleagues at Nichia Chemical Industries [39]. On the back of this development, the III-
The III-nitrides, like silicon carbide, exhibit both wurtzite and zinc blende polytypes. Some of the properties of the binary phase nitrides are summarised in Table 2. The difference between the melting points of AlN, GaN and InN and their dissociation temperature under atmospheric nitrogen means that single crystal growth cannot be achieved from stoichiometric melts as in the Czochralski or Bridgman methods. Furthermore crystallisation from solution requires very high over pressures of nitrogen to increase the concentration of nitrogen in the melt to be effective [40].

The lattice parameter difference between the wurtzite phases of Gallium nitride and aluminium nitride is only 2.4% and so may be co-deposited to form a continuous film on which the single crystal layer can be deposited and temperature forming an epitaxially oriented polycrystalline lateral growth. This layer is subsequently annealed at higher temperatures as high as 1500°C with room temperature mobilities as high as 1000 cm²/Vs. Given this characteristic of the GaN epilayers the successful development of p-type doping has been tortuous. Magnesium is an effective p-dopant in GaN [43]. Various means of optimising the activation coefficient have been pursued including low energy electron beam irradiation [44] or high temperature annealing (700°C) under nitrogen [45]. The acceptor is readily passivated by annealing in an ammonia at 700°C and is a reversible process [46].

Intentionally doped n-type GaN have been investigated using the incorporation of Si and Ge impurities [47]. Carrier concentrations were measured proportional to the feedstock gas flows of silane and germane in the deposition process. Silicon doped epilayers were produced with \( n = 10^{17} \text{ to } 10^{19} \text{ cm}^{-3} \) and germanium doped material exhibited carrier concentrations in the range \( 7 \times 10^{16} \text{ to } 10^{19} \text{ cm}^{-3} \). The activation coefficient of the Si donor was estimated to be an order of magnitude higher than germanium.

N-type doping of Al\(_{x}\)Ga\(_{1-x}\)N \((0.12 \leq x \leq 0.42)\) / 6H-SiC with Si has been demonstrated [48]. Undoped Al\(_{0.15}\)Ga\(_{0.85}\)N films deposited on vicinal 6H-SiC(0001) exhibited residual ionised donor concentrations of \( 1 \times 10^{16} \text{ cm}^{-3} \). The concentration dropped markedly with increasing Al content to less than \( 1 \times 10^{15} \text{ cm}^{-3} \) for Al\(_{0.35}\)Ga\(_{0.65}\)N. Using a silane source ionised donor concentrations in the range \( 2 \times 10^{17} \text{ to } 10^{19} \text{ cm}^{-3} \) for \( 0.12 \leq x \leq 0.42 \). Above \( x \approx 0.42 \) the films became too resistive to measure by capacitance-voltage techniques.

### 3.7 III-nitride based high temperature electronics

The application of III-nitrides in high temperature electronics have only recently begun to be explored. One study by Khan et al [49] reports the fabrication of a heterostructure field effect transistor (HFET) capable of operation at 300°C. The device geometry incorporated a 0.2 µm gate length AlGaN/GaN based structure using an aluminium nitride buffer layer on sapphire, a GaN channel and an n-Al\(_{0.35}\)Ga\(_{0.65}\)N spacer layer to control the device threshold voltage. The whole device was isolated on a mesa structure. The source-drain metalisation were titanium/ aluminium and the Schottky barrier metal was titanium for the gate. The transconductance of the device at 25°C was 23 mS/mm and 13 mS/mm at 300°C. The threshold voltages at these temperatures were -2.5 and -2.1 V, respectively.

Another notable device study has been reported by Panikov and co-workers [50]. They have fabricated a heterobipolar transistor based on gallium nitride and silicon carbide. The GaN–SiC heterojunction allows high injection efficiency, even at elevated temperatures. The authors claim a record current gain of ten million at room temperature, decreasing to 100 at 535°C. An Arrhenius plot of current gain versus inverse temperature, \( T \), yielded an activation energy of 0.43 eV corresponding to valence band barrier blocking of the escape of holes from the base to the emitter. This activation energy is approximately equal to the difference of energy gaps between GaN emitter and SiC base. The transistor was operated at high power without cooling and a power density of 30 kW/cm² was sustained.

### 4. Diamond

#### 4.1. CVD diamond growth and doping

Since the early 1980’s diamond film growth by chemical vapour deposition using hydrogen and hydrocarbon feedstocks has been widely investigated. In general films are polycrystalline on hetero substrates unless some form of buffer layer is employed such as the use of n-type enhanced...
nucleation [51] which has proved to be a significant development as it overcomes the requirement to form nucleation sites on substrates using mechanical abrasion and has enabled the deposition of heteroepitaxially oriented diamond on substrates such as silicon and silicon carbide [52].

X-ray diffraction measurements [53] of oriented diamond films deposited on silicon (100) and silicon (111) substrates using bias enhanced nucleation coupled with CVD growth process shows the epitaxial relationship between diamond and silicon, namely that the orientations are diamond (001)[110] || Si(001)[110] and diamond (111)[110] || Si(111)[110], respectively, to within a spread of a few degrees. Furthermore the orientation of the (111) films is closer than (100) oriented diamond but the twinning behaviour of CVD diamond on the (111) surface is a complication in epitaxial growth. Consequently there have been numerous studies made of diamond growth on silicon (100) in pursuit of ‘device quality’ material [54,55].

Another development in oriented diamond film growth was reported by Locher et al [56] who have identified the stabilisation of texturing growth conditions by the addition of nitrogen to hydrogen–methane diamond growth mixtures. For small partial pressures of methane the nitrogen additions had little effect however for methane fractions of between 1–2% additions of 10–100 ppm nitrogen altered the film morphology from a nanocrystalline structure to a pronounced (100) texture. Nitrogen concentrations in excess of 500 ppm caused the crystallinity to collapse into a nanostructure once more. Nitrogen incorporation is significantly larger on the [111] growth sector compared with the [100] sector and this may influence the competitive growth rates to favour one texture over another.

Boron is a substitutionally sited acceptor in diamond but it has a relatively high activation energy (365 meV) and the degree of thermal ionisation imposes limits on the doping regimes that can be employed for various applications. Various methods for doping CVD diamond films have been employed such as in situ doping [57], implantation [58] and diffusion. Generally polycrystalline diamond films contain high densities of electrically active defects which generates an intrinsic acceptor background concentration of $\sim 10^{15}$ cm$^{-3}$ eV$^{-1}$ at some 0.8 eV above the valence band closing rapidly to within 0.2 eV at $\sim 10^{18}$ cm$^{-3}$ eV$^{-1}$ [59] and they can be compensated by nitrogen impurities. Extrinsic p-type doping with boron is only achieved in the approximate concentration range $10^{15}–5 \times 10^{16}$ cm$^{-3}$ as shown in Fig. 2 [60]. Above $\sim 10^{15}$ B cm$^{-3}$ impurity band conduction occurs and the observed boron activation energy drops to the meV level.

Significant advances have been made over the last few years in the area of n-type doping of diamond. It has been demonstrated [61] that implantation of Li and Na into diamond generates electrically active dopants with activation energies of $\sim 0.2$ eV over the temperature range 100–380°C and shows a linear dependence of the log(resistance) versus $T^{1/4}$ which is indicative of a variable range hopping conduction mechanism. Phosphorous is also a candidate n-type dopant in diamond. Fig. 2 incorporates work from two studies made using phosphorus to achieve n-type conductivity [62,63] Nishimori et al [62] have used gas source molecular beam epitaxy to deposit phosphorus doped homoeptaxial diamond films from methane and tri-n-butylphosphine at 1000°C. They attribute the achievement of a room temperature conductivity of 0.33($\Omega$ cm)$^{-1}$ to the lack of hydrogen usually required by CVD diamond processes and they speculate that hydrogen passivation of P donors causes the lower conductivities observed in other phosphorus doping studies.

4.2. Diamond high temperature electronics

A range of diamond devices have been fabricated and characterised for use in high ambient temperatures or in high power applications where ohmic heating causes high junction temperatures. Examples of these devices include thermistors [64,65], pressure transducers [60,66], diodes [62,67] and transistors of various types [68–72].

Diamond metal-insulator-semiconductor field effect transistors (MISFETs) have been investigated using SiO$_2$ as the gate material [68,69] or by using an insulating diamond gate instead [70,71] which exhibits lower interface trap densities and gate leakage currents.

A particular example [72] of one of these devices is a depletion-mode MISFET which has been fabricated from thin film polycrystalline diamond with an insulating diamond gate. Ion implantation was used to define a boron...
doped p-type channel and ohmic contact regions. Gold and
gold–silver–titanium metallisation schemes were used for
the gate and source-drain contacts, respectively. For high
temperature operation, MISFETs are required to minimise
gate leakage currents and this device was successfully oper-
ated at 300°C displaying pinch off when in depletion with
high levels of channel current modulation in enhancement.
A transconductance value of 174 mS/mm was reported
which is still believed to be the highest value to date for
this type of device.

5. Conclusions

During the last decade growth processes for the wide
bandgap semiconductors reviewed here have advanced
significantly to the point where defect concentrations are
low enough to enable credible high temperature demon-
strator devices to be fabricated. The device concepts that have
been explored illustrate that most of the processing issues
have been addressed to some extent however on-going
formation schemes for ohmic and rectifying contacts; formation of
gate dielectrics; and delineation processes such as selective
deposition or etching.

The specific issues for wide bandgap high temperature
electronics will continue to be the identification of material
systems which are stable against corrosion or diffusion. The
likely applications for wide bandgap semiconductor devices
is beyond the scope of this paper. However it is likely that
they will be used where silicon or gallium arsenide cannot,
that is above 300–400°C. This temperature regime is the
domain of microsystem technologies for intelligent distributed
control systems where a wide range or sensor or actua-
tion functions are required.

References

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