8284A Clock Generator: -

→ The 8284A is an ancillary component to the 8086/8088 microprocessors. Without the clock generator, many additional circuits are required to generate the clock (CLK) in an 8086/8088-based system.

→ The 8284A provides the following basic functions or signals:
  → Clock generation (CLK)
  → RESET synchronization
  → READY synchronization
  → TTL level peripheral clock (PCLK)

<table>
<thead>
<tr>
<th>Pins</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>AEN1 and AEN2 (Address enable)</td>
<td>Used to cause wait states, along with the RDY1 and RDY2 inputs. Wait states are generated by the READY pin of the 8086/8088 microprocessors, which is controlled by these two pins (inputs).</td>
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<tr>
<td>RDY1 and RDY2 (Bus ready)</td>
<td>Provided in conjunction with AEN1 and AEN2 to cause wait states in an 8086/8088-based system.</td>
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<tr>
<td>ASYNC (Ready synchronization)</td>
<td>The ready synchronization selection input selects either one or two stages of synchronization for the RDY1 and RDY2 inputs.</td>
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<tr>
<td>READY</td>
<td>READY is an output pin that connects to the 8086/8088 READY input. This signal is synchronized with the RDY1 and RDY2 inputs.</td>
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<tr>
<td>X1 and X2 (Crystal inputs)</td>
<td>An external crystal oscillator is connected to these inputs.</td>
</tr>
<tr>
<td>F/C (Frequency/Crystal select)</td>
<td>=1, an external clock is provided to the EFI input pin. =0, an external crystal oscillator connected to X1 and X2 provides the clock.</td>
</tr>
<tr>
<td>EFI (External Frequency Input)</td>
<td>Supplies the timing whenever the F/C is high.</td>
</tr>
<tr>
<td>CLK (Clock)</td>
<td>Provides CLK input signal to the 8086/8088 microprocessors and other components in the system. ( f_{\text{clk}} = \frac{1}{3} \left( f_{\text{crystal/EFI}} \right) ), Duty cycle = 33% which is required by 8086/8088.</td>
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<tr>
<td>PCLK (Peripheral clock)</td>
<td>Provides clock signal to peripheral devices (slower as compare to microprocessor). ( f_{\text{PCLK}} = \frac{1}{6} \left( f_{\text{crystal/EFI}} \right) ), Duty cycle = 50%.</td>
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<tr>
<td>OSC (Oscillator)</td>
<td>TTL level signal output. Provides an EFI input to other 8284A clock generators in some multiple processor systems.</td>
</tr>
<tr>
<td>RES (Reset input)</td>
<td>Active low input. Often connects to an RC network that provides power-on resetting.</td>
</tr>
<tr>
<td>RESET (Reset output)</td>
<td>Connects to the 8086/8088 RESET input pin.</td>
</tr>
<tr>
<td>CSYNC (Clock synchronization)</td>
<td>Used whenever the EFI input provides synchronization in systems with multiple processors. If the internal crystal oscillator is used, this pin must be grounded.</td>
</tr>
<tr>
<td>GND</td>
<td>Connects to ground.</td>
</tr>
<tr>
<td>Vcc</td>
<td>Connects to +5.0V with a tolerance of ±10 percent.</td>
</tr>
</tbody>
</table>
Bus Cycle: -

- Bus Cycle defines the basic operation that a microprocessor performs to communicate with external devices.
- Bus Cycle is the period of time in which 8086/8088 microprocessors uses the memory and I/O.
- Each Bus Cycle equals four system clocking periods (T states).
- These four clocking periods are denoted as T1, T2, T3 and T4.

During T1:
- The address of the memory or I/O location is sent out via the address/data bus connections.
- Control signals ALE, DT/R and IO/M (8088) or M/IO (8086) are generated.
- The IO/M or M/IO signal indicates whether the address bus contains a memory address or an I/O device (port) number.

During T2:
- The 8086/8088 microprocessor issue the RD or WR signal, DEN and in the case of a write, the data to be written appears on the data bus. These events cause the memory or I/O device to begin to perform a read or write. DEN signal turns on the data bus buffers, if they are present in the system.
- So, for read operation microprocessor can accept the data read from the memory or I/O and the data are sent out to the memory or I/O through the data bus in write bus cycle.

During T3:
- READY is sampled at the end of T2. If READY is low at this time, T3 becomes a wait state (Tw). This clocking period is provided to allow the memory time to access data. If this bus cycle is happened to be a read bus cycle, the data bus is sampled at the end of T3.

During T4:
- All bus signals are deactivated in preparation for the next bus cycle. This is also the time when the 8086/8088 microprocessors sample the data bus connections for data that are read from memory or I/O.
- Also the trailing edge of the WR signal transfers data to the memory or I/O, which activates and writes when the WR signal returns to a logic 1 level.

Bus Cycles of 8086/8088: -
- The bus cycles present in 8086/8088 are:
  - Opcode fetch
  - Memory read
  - Memory write
  - I/O read
  - I/O write
  - Interrupt acknowledge
Bus Buffering and Latching: -

→ In any microprocessor based system the multiplexed buses must be demultiplexed first.
→ The address/data bus on the 8086/8088 is multiplexed (shared) to reduce the numbers of pins required for the 8086/8088 integrated circuit.
→ Demultiplexing is required because memory and I/O require that the address remains valid and stable throughout a read or write cycle. If the buses are multiplexed, the address changes at the memory and I/O, which causes them to read or write data in the wrong locations.
→ There are three types of buses present in any microprocessor system for interfacing memory and I/O with microprocessor.
   → Address Bus: provides the memory and I/O with the memory address or the I/O port number.
   → Data Bus: transfers data between the microprocessor and the memory or I/O in the system.
   → Control Bus: provides control signals to the memory and I/O.

Buffering the system:

→ For very large systems where more than 10 units load is attached to any bus pin, the entire 8086/8088 system must be buffered. Buffering is used to enhance output currents so that more TTL unit loads may be driven.
→ A fully buffered signal introduces a timing delay to the system. This causes no difficulty unless memory or I/O devices are used, which function at near the maximum speed of the bus.

Latching the address bus:

→ For getting the whole 20 bit address available during a bus cycle, we have to use latches with the multiplexed address/data bus.
→ Whenever the address latch enable (ALE) pin becomes a logic 1, a latch pass the inputs to the outputs. After a short time, ALE returns to its logic 0 condition, which causes the latches to remember the inputs at the time of the change to a logic 0.

READY and Wait State: -

→ Causes wait states for slower memory and I/O components. A wait state (Tw) is an extra clocking period, inserted b/w T2 and T3, that lengthens the bus cycle. If one wait state is inserted then the memory access time, normally 460nsec with a 5MHz clock, is lengthened by one clocking period (200nsec) to 660nsec.
→ READY is sampled at the end of T2 and again, if applicable in the middle of Tw.
→ If READY is 0, Tw is sampled between T2 and T3.
→ READY is tested for a logic 0 on the 1 to 0 transition of the clock at the end of T2 and for a logic 1 on the 0 to 1 transition of the clock in the middle of Tw.
Minimum Mode Operation: -
→ All the control signals for the memory and I/O are generated by the microprocessor, so it costs less.

Maximum Mode Operation: -
→ There are not enough pins on the 8086/8088 for bus control during maximum mode because new pins and new features have replaced some of them.
→ Some of the control signals must be externally generated. This requires the addition of an external bus controller- the 8288 bus controller.
→ Maximum mode is used only when the system contains external coprocessors such as the 8087 arithmetic coprocessor.